IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:)	
Benjamin S. Ting) Examiner:	Not yet assigned
Application No.: Not yet assigned) Art Unit:	Not yet assigned
Filed: Herewith)	
For: ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS))))	
a Continuation of)	
Application No.: 10/428,724)	
Filed: May 1, 2003)	
	 /	

Commissioner for Patents PO Box 1450 Alexandria, Virginia 22313-1450

NOTICE OF INTERFERENCE

Sir:

<u>-</u>

This is to notify the Examiner of an Interference No. 103,833 with respect to U.S. Patent No. 5,457,410, a patent related to the present application.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 4/2/, 2004

Daniel E. Ovanezian

Registration No. 41,236

12400 Wilshire Boulevard Seventh Floor Los Angeles, CA 90025-1026 (408) 720-8300

"Express Mail" mailing label number: EV409358900US
Date of Deposit: 4/21/04
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post
Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to Commissioner f
Patents, PO Box 1450, Alexandria, Virginia 22313-1450
JUANITA BRISCOE
(Typed or printed name of person mailing paper or fee)
(Signature of person mailing paper or fee)
4/21/04
(Date signed)

.